Dr. Richa Gupta
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CURRENT POSITION

Assistant Professor, J& K Higher Education Department

CURRENT POSTING

Department of Electronics, GGM Science College, Jammu (since 01.08.2024)

RESEARCH EXPERIENCE

5+ years (after PhD)

PREVIOUS EMPLOYMENT

Lecturer (Contractual) in Department of Electronics, University of Jammu (from 23.08.2019 to 18.01.2023)

RESEARCH WORK

Field of Research Interest: Device Simulation and Fabrication of Nano-scale devices.

Ph.D. (Awarded in 2019)
Title of Ph.D. Thesis: Study of High-k materials for Nano scale devices and their applications.

M.Phil. (Awarded in 2014)\
Title of M.Phil Dissertation: Investigating Si/InAs as Channel Material for Gate All Around Nanowire FET

Research Publications 11 (For Details Kindly Refer Annexure - I)

Conferences/Seminars 15 (For Details Kindly Refer Annexure – II)

Book Chapters 03 (For Details Kindly Refer Annexure – III)

Workshops Attended 05 (For Details Kindly Refer Annexure – IV)

ACADEMIC QUALIFICATIONS

- **Ph.D. in Electronics** from University of Jammu (2019)
- **M. Phil in Electronics** from University of Jammu (2014)
- **Post Graduation** (M.Sc.) in Electronics from University of Jammu, Jammu (J&K), India (2011)
- **Graduation** (B.Sc.) with Mathematics, Physics, Chemistry from Govt. Degree College, Kathua, J&K (2009)
- **12th** (Mathematics, Physics, Chemistry) from Shakti Modern Higher Secondary School, Kathua, J&K, India (2006)
- **10th** (Mathematics, Physics, Chemistry, Biology) from Shakti Modern Higher Secondary School, Kathua, J&K, India (2004)

TECHNICAL SKILLS

Languages : Basics of C++

IDE/Tools : MS Word, MS Excel, MS PowerPoint.

ACHIEVEMENTS

- Qualified National Eligibility Test (NET) conducted by University Grants Commission (UGC), June 2013.
- Qualified for the Award of **Junior Research Fellowship (JRF)** by CBSE-UGC-NET, December 2014.
- Qualified for the Award of **UGC Senior Research Fellowship (SRF)**, June 2017.
- Project entitled **"To fabricate and study the electrical characteristics of Pt/TiO_2/Au/SiON/Si structure employing metal nano-dots for non-volatile memory applications"** successfully completed at **Indian Institute of Technology Bombay (IITB)** w.e.f. March-July, 2015 under **INUP** scheme.
- Guided students pursuing M.Sc. and M. Tech. in their research work during my Ph.D. and teaching tenure in University of Jammu.

Declaration:

I hereby declare that the above-mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.

Date: 02 August, 2024 ***Dr. Richa Gupta***

Place: Jammu

ANNEXURE I

RESEARCH PUBLICATIONS

1. **Richa Gupta** and Rakesh Vaid, "Structural and Electrical Characteristics of ALD TiO_2/SiON/n-Si Gate-Stack for Advanced CMOS Device Applications" published in **IEEE Transactions on Electron Devices** (Early Access), DOI: 10.1109/TED.2021.3075394

2. **Richa Gupta** and Rakesh Vaid, "TCAD Performance Analysis of High-K dielectrics for Gate All Around InAs Nanowire Transistor Considering Scaling of Gate Dielectric Thickness" **Microelectronic Engineering (Elsevier)**, vol. 160, pp. 22-26, 2016.

3. **Richa Gupta,** Renu, Rakesh Prasher and Rakesh Vaid, "Structural and Electrical characteristics of ALD-HfO_2/n-Si Gate stack with SiON Interfacial layer for advanced CMOS Technology", **Solid State Sciences (Elsevier)**, vol. 59, pp. 7-14, 2016.

4. **Richa Gupta** and Rakesh Vaid, "Effect of Post Deposition Annealing on ALD-ZrO_2/SiON Gate Stacks for Advanced CMOS Technology", **ECS Transactions**, vol. 75, Issue 17, pp. 67-73, 2016.

5. **Richa Gupta**, Dulen Saikia and Rakesh Vaid, "Argon Annealed ALD-ZrO_2/ SiON Gate Stack for Advanced CMOS Devices", **ECS Transactions**, vol.77, Isuue 5, pp. 51-55, 2017.

6. Renu Rajput, **Richa Gupta**, Rakesh K. Gupta and Ajit Khosla and Rakesh Vaid, "Fabrication and characterization of n-Si/SiON/metal gate structure for future MOS technology", Microsystem Technologies **(Springer)**, 2018.

7. **Richa Gupta** and Rakesh Vaid, "Structural and Electrical Characteristics of Oxygen Annealed ALD-ZrO_2/SiON Gate Stack for Advanced CMOS Devices", **ECS Transcations**, vol. 85, Issue 13, pp. 1481-1487, 2018.

8. **Richa Gupta,** Renu and Rakesh Vaid, "Fabrication and Characterization of Ti-Pt/HfO_2/SiO_2~4.5nm/n-Si Nanoscale Device for Advanced CMOS Applications", International Journal of Scientific and Technical Advancements, vol.1, Issue 3, pp. 77-81, 2015 [ISSN: 2454-1532].

9. Vinay Kumar, **Richa Gupta**, Raminder Preet Pal Singh, Rakesh Vaid, "Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials" International Journal of Innovative Research in Science, Engineering and Technology", vol. 5, Issue 7, July 2016 [ISSN(Online): 2319-8753 ISSN (Print): 2347-6710][DOI:10.15680/IJIRSET.2016.0507090].

10. Renu, **Richa Gupta** and Rakesh Vaid, " Electrical characterization of metal gate MOScap with ultrathin silicon oxide as gate dielectric", International Journal of Scientific and Technical Advancements, Volume 1, Issue 3, pp. 51-54, 2015 [ISSN: 2454-1532].

11. Vinay kumar, Raminder Preet Pal Singh, **Richa Gupta**, Rakesh Vaid, "Effect of High-k Gate Dielectric Materials on Electrical characteristics of GaAs Channel Material Based Double Gate n-FinFET", International Journal of Emerging Research in Management &Technology, vol. 5, Issue 8, 2016 [ISSN: 2278-9359].

ANNEXURE II

CONFERENCES/SEMINARS

1. Rakesh Vaid and **Richa Gupta**, "Fabrication and Characterization of High-k Dielectrics Based Gate Stacks/MOS Capacitors for Advanced CMOS Devices", in the proceedings of **IEEE 31st International Conference on Microelectronics (MIEL)** held in **Serbia**, pp. 75-78, 2019.

2. **Richa Gupta**, Devi Dass, Rakesh Prasher and Rakesh Vaid, "Study of Gate all around InAs/Si based Nanowire FETs using Simulation Approach", in proceedings of IEEE International Conference on Signal Propagation and Computer Technology **(IEEE-ICSPCT)** held at Ajmer, pp. 557-560, 2014.

3. **Richa Gupta**, Devi Dass, Rakesh Prasher and Rakesh Vaid, "Impact of Silicon Body Thickness on the Performance of Gate-All-Around Silicon Nanowire Field Effect Transistor" in the proceedings of Environmental Science and Engineering **(Springer)**, pp. 689-692, 2014 [ISSN 1863-5539].

4. **Richa Gupta**, Deepika Jamwal and Rakesh Vaid, "Impact of Body Thickness on the Performance of InAs Gate-all-around Nanowire Field Effect Transistor" in proceedings of International Conference on Advances in Computers, Communication and Electronic Engineering held at University of Kashmir, March 16-18, 2015.

5. Deepika Jamwal, **Richa Gupta** and Rakesh Vaid, "Impact of Scaling Gate Oxide thickness on the performance of Silicon based Triple gate/Quad gate Rectangular-NWFET" in proceedings of International Conference on Advances in Computers, Communication and Electronic Engineering held at University of Kashmir, March 16-18, 2015.

6. **Richa Gupta** and Rakesh Vaid, "Fabrication and Characterization of high-k based nano-MOS capacitors for advanced CMOS applications" presented in "National seminar cum workshop on advances in science and technology and pertinent need of instrumentation" held at Department of Physics and IQAC Sibsagar College, Joysagar, w.e.f. 9th-10th September, 2016.

7. **Richa Gupta** and Rakesh Vaid, "Study of Electrical properties of Si based double gate n-finfet employing HfO_2 and La_2O_3 as high-k dielectrics" presented in "4th J&K women science congress' w.e.f. I st-3rd September, 2016.

8. Presented a research paper entitled "Comparative Study of Gate All Around InAs NWFET and Si NWFET for Gate Dielectric Thickness", **Richa Gupta**, Deepika Jamwal and Rakesh Vaid, in 101st Indian Science Congress-2014, held at University of Jammu, Jammu.

9. Presented a research paper entitled "Performance analysis of Ti-Pt/HfO_2/Si Nano-MOS Employing Silicon Oxynitride as interfacial layer" **Richa Gupta**, Renu and Rakesh Vaid, in 18th International Workshop on Physics of Semiconductor Devices (IWPSD) held at Indian Institute of Bangalore, 2015.

10. Presented a research paper entitled "Scaling Effect of gate insulator thickness on the performance of Silicon Metal Oxide Semiconductor Capacitor" **Richa Gupta**,

Deepika Jamwal and Rakesh Vaid, presented a paper in NISS National Symposium held at GGM Science College, Jammu w.e.f. Feb. 27-28, 2015.

11. Presented a research paper entitled "Fabrication and Characterization of Ti-Pt/HfO_2/SiO_2~4.5nm/n-Si Nanoscale Device for Advanced CMOS Applications", **Richa Gupta**, Renu and Rakesh Vaid in 3rd National Conference & Exhibition on Emerging & Innovative Trends in Engineering Technology (NCEEITET) held at GCET Jammu w.e.f. September 15-16, 2015.

12. Presented a research paper entitled "Emerging high-k dielectrics for advanced MOS capacitor applications", **Richa Gupta**, Deepika Jamwal and Rakesh Vaid in the National Conference on Trends in Electronics and Computational technologies (NCTECT) held at University of Jammu, Jammu w.e.f. March 20, 2015.

13. Deepika Jamwal, **Richa Gupta** and Rakesh Vaid, "A Review on the Silicon based Solar cell", poster presentation in the National Conference on Trends in Electronics and Computational technologies (NCTECT) held at University of Jammu, Jammu w.e.f. March 20, 2015.

14. Deepika Jamwal, **Richa Gupta** and Rakesh Vaid, "Comparative study of silicon based triple gate and quad gate rectangular-NWFET on its device metrics by scaling channel width" poster presentation in NISS National Symposium held at GGM Science College, Jammu, Feb. 27-28, 2015.

15. Presented a research paper entitled "Impact of nitrogen annealing on the performance of SiON based nano-MOS employing bilayer metal gate" **Richa Gupta** and Rakesh Vaid, in National conference on Role of Mathematics and Computer Science in Advancement of Physics held at GDC Kathua w.e.f. 26-27, February, 2016.

ANNEXURE III

BOOK CHAPTERS

S.No.	Chapter Title	Author	Status
1.	Impact of Silicon Body Thickness on the Performance of Gate-all-around Silicon Nanowire Field Effect Transistor	1st	Book chapter: Physics of Semiconductor Devices (Springer)
2.	Applications of Nanoscale Devices in Circuits	1st	Book chapter: In Micro and Nano Technologies, Nanoelectronics: Physics, Materials and Devices, Elsevier
3.	Physical Properties of Carbon Nanotubes and Nanoribbons	2nd	Book chapter: In Woodhead Publishing Series in Electronic and Optical Materials, Graphene, Nanotubes and Quantum Dots-Based Nanotechnology

ANNEXURE IV

WORKSHOPS ATTENDED

1. Attended INUP Hands-on-training workshop on Fabrication of MEMS Sensor held at IITB w.e.f. March 23-27, 2015.
2. Attended INUP Familiarization Workshop on Nanofabrication Technologies w.e.f. May 26-28, 2014.
3. Attended 2-day Familiarization Workshop on Nanofabrication Technologies w.e.f. Sept. 6-7, 2014.
4. Attended 2-day National Workshop on Advances in Interdisciplinary Sciences w.e.f. 11-12, 2018.
5. Attended 3-day Workshop on 'Internationalization of Higher Education: Opportunities and Challenges' held at University of Jammu w.e.f w.e.f. 16-18, 2023.